

THE CLAIMS

1. (Currently Amended) An information processing apparatus comprising:

a clock generating circuit generating an internal clock signal having a frequency which is the same as or is a multiple ratio of a frequency of a reference clock signal by changing an oscillating cycle of a clock signal; and

5 a control circuit setting a first initial value in said clock generating circuit on the basis of a first instruction from the outside, wherein

said clock generating circuit includes a multiplication circuit, and said multiplication circuit includes:

10 a first counter receiving said first initial value from said control circuit, adjusting a first count value to specify said oscillating cycle of said clock signal by using said first initial value as a first initial count value, and outputting said first count value; and

an oscillation circuit receiving said first count value from said first counter and oscillating said clock signal on the basis of said first count value.

2. (Original) The information processing apparatus according to claim 1, wherein

at the time of system activation or reset, said control circuit sets a predetermined count value, which is prestored, as said first initial value into said first counter.

3. (Original) The information processing apparatus according to claim 1, wherein

when said clock generating circuit stops and, then, operates again, said control circuit sets said first count value read from said first counter before the stop as said first initial value into said first counter.

4. (Original) The information processing apparatus according to claim 1, wherein
when the frequency of said reference clock signal is changed, said control circuit calculates said first initial value on the basis of said first count value read from said first counter before the change and the frequencies of said reference clock signal before and after the change,
5 and sets said calculated first initial value into said first counter.

5. (Original) The information processing apparatus according to claim 1, wherein
when a multiple ratio between said reference clock signal and said internal clock signal is changed, said control circuit calculates said first initial value on the basis of said first count value read from said first counter before the change and said multiple ratio before and after the change,
5 and sets said calculated first initial value into said first counter.

6. (Original) The information processing apparatus according to claim 1, further comprising:

a detection circuit detecting that said first count value of said first counter lies out of a predetermined range and notifying said control circuit of a detection result, wherein

5 said control circuit uses, in response to receiving signal detection result, said reference clock signal in place of said internal clock signal as an operation clock signal of the information processing apparatus.

7. (Original) The information processing apparatus according to claim 6, wherein said detection circuit notifies of said detection result to the outside.

8. (Original) The information processing apparatus according to claim 1, further comprising:

a detection circuit detecting that said first count value of said first counter lies out of a predetermined range and notifying said control circuit of a detection result, wherein

5 said control circuit, in response to receiving said detection result, changes a multiple ratio between said reference clock signal and said internal clock signal so that said first count value lies within said predetermined range.

9. (Original) The information processing apparatus according to claim 1, further comprising

a pulse counter counting the number of pulses of said clock signal, wherein

5 said control circuit calculates said first initial value on the basis of a pulse count value counted by said pulse counter in a predetermined period and sets said calculated first initial value into said first counter.

10. (Original) The information processing apparatus according to claim 9, further comprising:

a storage circuit storing data, wherein

said control circuit writes said calculated first initial value into said storage circuit and, at
5 the time of system activation or reset, sets said first initial value read from said storage circuit
into said first counter.

11. (Original) The information processing apparatus according to claim 9, further
comprising:

a fuse circuit including a fuse element, wherein

said fuse element in said fuse circuit is disconnected on the basis of said pulse count
5 value, and

at the time of system activation or reset, said control circuit calculates said first initial
value on the basis of said pulse count value determined on the basis of a disconnection state of
said fuse element.

12. (Original) The information processing apparatus according to claim 1, wherein
said clock generating circuit further includes a phase synchronization circuit
synchronizing a phase of said internal clock signal with a phase of said reference clock signal,
said control circuit further sets a second initial value into said phase synchronization

5 circuit on the basis of a second instruction from the outside, and

said phase synchronization circuit includes:

a phase comparator comparing said phase of said internal clock signal with said phase of
said reference clock signal;

a second counter receiving a phase comparison result and said second initial value from
10 said phase comparator and said control circuit, respectively, adjusting a second count value to

specify a delay amount of said clock signal received from said oscillation circuit by using said second initial value as a second initial count value on the basis of said phase comparison result, and outputting said second count value; and

15 a variable delay circuit receiving said second count value from said second counter, delaying said clock signal received from said oscillation circuit on the basis of said second count value, and outputting said internal clock signal.

13. (Original) The information processing apparatus according to claim 12, wherein at the time of system activation or reset, said control circuit sets a predetermined count value, which is prestored, as said second initial value into said second counter.

14. (Original) The information processing apparatus according to claim 12, wherein when said clock generating circuit stops and, then, operates again, said control circuit sets said second count value read from said second counter before the stop as said second initial value into said second counter.

15. (Original) The information processing apparatus according to claim 12, further comprising:

5 another clock generating circuit generating another internal clock signal having a frequency which is the same as or is a multiple of the frequency of said reference clock signal by changing an oscillating cycle of another clock signal, wherein said control circuit further sets third and fourth initial values into said another clock generating circuit on the basis of third and fourth instructions, respectively, from the outside,

said another clock generating circuit includes:

10 a third counter receiving said third initial value from said control circuit, adjusting a third count value to specify said oscillating cycle of said another clock signal by using said third initial value as a third initial count value, and outputting said third count value;

another oscillation circuit receiving said third count value from said third counter and oscillating said another clock signal on the basis of said third count value; and

15 another phase synchronization circuit synchronizing a phase of said another internal clock signal with a phase of said reference clock signal, and

said another phase synchronization circuit includes:

another phase comparator comparing said phase of said another internal clock signal with said phase of said reference clock signal;

20 a fourth counter receiving a phase comparison result and said fourth initial value from said another phase comparator and said control circuit, respectively, adjusting a fourth count value to specify a delay amount of said another clock signal received from said another oscillation circuit by using said fourth initial value as a fourth initial count value on the basis of said phase comparison result, and outputting said fourth count value; and

25 another variable delay circuit receiving said fourth count value from said fourth counter, delaying said another clock signal received from said another oscillation circuit on the basis of said fourth count value, and outputting said another internal clock signal, and

when an operation setting of said another clock generating circuit is changed to the same condition as that of said clock generating circuit, said control circuit calculates said third initial value after the change on the basis of said first count value read from said first counter before the
30 change, sets said calculated third initial value into said third counter, and sets said second count

value read from said second counter before the change as said fourth initial value into said fourth counter.

16. (Original) The information processing apparatus according to claim 1, further comprising:

another clock generating circuit generating another internal clock signal having a frequency which is the same as or is a multiple of the frequency of said reference clock signal by changing an oscillating cycle of another clock signal, wherein

said control circuit further sets a second initial value into said another clock generating circuit on the basis of a second instruction from the outside,

said another clock generating circuit includes:

a second counter receiving said second initial value from said control circuit, adjusting a second count value to specify said oscillating cycle of said another clock signal by using said second initial value as a second initial count value, and outputting said second count value; and

another oscillation circuit receiving said second count value from said second counter and oscillating said another clock signal on the basis of said second count value, and

when an operation setting of said another clock generating circuit is changed to the same condition as that of said clock generating circuit, said control circuit calculates said second initial value after the change on the basis of said first count value read from said first counter before the change and sets said calculated second initial value into said second counter.

17. (Original) An information processing apparatus comprising:

a clock delay circuit delaying a first clock signal to synchronize said first clock signal with a second clock signal; and

a control circuit setting an initial value in said clock delay circuit on the basis of a first instruction from the outside, wherein

said clock delay circuit includes:

a phase comparator comparing a phase of said first clock signal with a phase of said second clock signal;

a counter receiving a phase comparison result and said initial value from said phase comparator and said control circuit, respectively, adjusting a count value to specify a delay amount of said first clock signal by using said initial value as a first initial count value on the basis of said phase comparison result, and outputting said adjusted count value; and

a variable delay circuit receiving said count value from said counter and delaying said first clock signal on the basis of said count value.

18. (Original) The information processing apparatus according to claim 17, wherein when said clock delay circuit stops and, then, operates again, said control circuit sets said count value read from said counter before said clock delay circuit stops as said initial value into said counter.

19. (Original) The information processing apparatus according to claim 17, wherein when a load capacity of a load circuit changes and, then, returns to the state before the change, said control circuit sets said count value read from said counter before the change as said initial value into said counter.

20. (Currently Amended) The information processing apparatus according to claim 17, further comprising:

another clock delay circuit delaying a third clock signal to synchronize said third clock signal with a fourth clock signal, wherein

5 said control circuit further sets another initial value in said another clock delay circuit on the basis of a second instruction from the outside,

said another clock delay circuit includes:

another phase comparator comparing a phase of said third clock signal with a phase of said fourth clock signal;

10 another counter receiving a phase comparison result and said another initial value from said another phase comparator and said control circuit, respectively, adjusting another count value to specify a delay amount of said third clock signal by using said another initial value as a second initial count value on the basis of said phase comparison result, and outputting said adjusted another count value; and

15 another variable delay circuit receiving said another count value from said another counter and delaying said third clock signal on the basis of said another count value, and

when an operation setting of said another clock delay circuit is changed to the same condition as that of said clock delay circuit, said control circuit sets said count value read from said counter before the change as said another initial value into said another counter.